This volume contains papers presented at The 2007 International Conference on Engineering of Reconfigurable Systems & Algorithms (ERSA'07). Their inclusion in this publication does not necessarily constitute endorsements by editors or by the publisher.

Copyright and Reprint Permission

Copying without a fee is permitted provided that the copies are not made or distributed for direct commercial advantage, and credit to source is given. Abstracting is permitted with credit to the source. Please contact the publisher for other copying, reprint, or republication permission.

Copyright © 2007 CSREA Press
ISBN: 1-60132-026-4
Printed in the United States of America
ERSA’07
ENGINEERING OF RECONFIGURABLE SYSTEMS AND ALGORITHMS

The international conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) was founded in 2001 and, since then, has been held each year in Las Vegas. The predecessor of ERSA was a workshop on Engineering of Reconfigurable Hardware/Software Objects (ENREGLE), which was hold at Las Vegas two years, since 1999.

During this period, the reconfigurable computing has gained more and more attention. In the early years the reconfigurable computing platform was used in very dedicated, specific application areas, in specialised signal and image processing systems and for prototyping VLSIs for embedded systems. On present days, the reconfigurable computing platform is used for a wide range of applications: from very dedicated embedded applications to supercomputing. The range of problems runs from purely hardware related designs to building multiprocessing systems and operating systems for reconfigurable spaces of elementary processors. The interests of researchers move from fine grain granularity and/or parallelism to coarse grain parallelism. The interest moves from physical level to abstract level, from physical placement to building flexible and configurable/adaptable multiprocessing environments.

ERSA conference solicits papers from all aspects of reconfigurable computing, including classical programmable logic, as well as configurable multiprogramming related papers. The topics of interests include theory, architecture, algorithms, design systems and applications that demonstrate the benefits of reconfigurable computing.

I would like to thank the authors for submitting their papers to ERSA’07 and for preparing the final versions of their papers for due date. I hope you all will have successful and enjoyable meeting in Las Vegas this year and I hope to meet you again in next years. I would like to extend my deepest gratitude for the efforts extended by the ERSA’07 Program Committee and to all external reviewers for their careful reading of all of the submitted papers.

Last but not least, I would like to thank the organizing team of The 2007 World Congress in Computer Science, Computer Engineering, and Applied Computing, and, especially, the General Chair Prof. Hamid Arabnia, for the continuous support and help in organizing the ERSA conference.

Toomas P. Plaks
ERSA Chair
London
April, 2007
ERSA’07 Conference Organisation

Conference Chair
Dr. Toomas P. Plaks
*London & Reading Univ., UK*

Advisory Board
Prof. Donald Bouldin
*Univ. of Tennessee, Knoxville USA*

Prof. Viktor K. Prasanna
*Univ. of Southern California USA*

Dr. Nick Tredennick
*Gilder Technology Report USA*

Steering Committee
Peter Athanas *Virginia Tech., USA*
Wayne Luk *Imperial College, UK*
Bernard Pottier *Univ. of Bretagne Occidentale, France*

Executive Committee
Ronald DeMara *Univ. of Central Florida, USA*
Steven Guccione *CMPWare, USA*

Programme Committee
Mahmoud Alahmad *University of Nebraska-Lincoln, USA*
David Andrews *Univ. of Kansas, USA*
Peter Athanas *Virginia Tech., USA*
Paul Beckett *RMIT Univ., Australia*
Donald Bouldin *Univ. of Tennessee, Knoxville, USA*
Timo Bretschneider *Nanyang Technological Univ., Singapore*
Gabriel Caffarena *Technical Univ. of Madrid, Spain*
Sek Chai *Motorola, USA*
Ronald DeMara *Univ. of Central Florida, USA*
Christopher Doss *North Carolina A & T State Univ., USA*
Antonio Gentile *Univ. of Palermo, Italy*
Guy Gogniat *Univ. of Bretagne Sud, France*
Marek Gorgo’n *AGH Univ. of Technology, Poland*
Steven Guccione *Cmpware, Inc., USA*
Frank Hannig *Univ. of Erlangen-Nürnberg, Germany*
Jim Harkin *University of Ulster, Northern Ireland*
Martin Herbordt *Boston Univ., USA*
Christian Hochberger *TU Dresden, Germany*
Xinming Huang *Univ. of New Orleans, USA*
Esther Hughes *Virginia Commonwealth Univ., USA*
Contents

SESSION: KEYNOTES AND INVITED TALKS

Challenges in Consumer Electronics for the 21st Century 3
Steven Leibson

Scientific Computing using Reconfigurable Hardware 13
Viktor Prasanna

A Unified Retargetable Design Methodology for Dedicated and Re–Programmable Multiprocessor Arrays: Case Study and Quantitative Evaluation 14
Juergen Teich, Frank Hannig, Holger Ruckdeschel, Hritam Dutta, Dmitrij Kissler, Andrej Stravet

An Integrated Platform for Heterogeneous Reconfigurable Computing 25
Bernard Pottier

SESSION: RECONFIGURABLE SYSTEMS ON CHIP

Swathi T. Gurumani, B. Earl Wells

Memory Hierarchy for MCSoPC Multithreaded Systems 44
Erik Anderson, Wesley Peck, Jim Stevens, Jason Agron, Fabrice Baijot, Seth Warn, David Andrews

Design Space Exploration of Multiprocessor Systems with MultiContext Reconfigurable Co–Processors 51
Pranav Vaidya, Jaehwan John Lee

Energy–Aware System Synthesis for Reconfigurable Chip Multiprocessors 61
Xiaofang Wang, Sotirios Ziavras, Jie Hu

SESSION: TASK SCHEDULING AND DYNAMIC RECONFIGURATION

HW implementation of an execution manager for reconfigurable systems 71
Javier Resano, Juan Antonio Clemente, Carlos Gonzalez, Jose Luis Garcia, Daniel Mozos

Task Partitioning for the Scheduling on Reconfigurable Systems driven by Specification 78
Self–Similarity
Matteo Giani, Massimo Redaelli, Marco Domenico Santambrogio, Donatella Sciuto

Configuration and Data Scheduling for Executing Dynamic Applications onto Multi−Context Reconfigurable Architectures 85
Fredy Rivera, Marcos Sanchez−Elez, Nader Bagherzadeh

A Compiler to Generate Hardware from Java Byte Codes for High Performance, Low Energy Embedded Systems 92
Darrin Hanna, Michael DuChene, Lawrence Kennedy, Brian Carpenter

Selecting Heterogeneous Computation Blocks for Reconfigurable JPEG Codec Computing 99
Wei−Ting wang, Wai−Hong Tam, Yi−Chi Chen, Kuen−Cheng Chiang, Chung−Ping Chung

SESSION: APPLICATIONS

High−Precision BLAS on FPGA−enhanced Computers 107
Chuan He, Guan Qin, Richard Ewing, Wei Zhao

High−efficiency protection solution for off−chip memory in embedded systems 117
Romain Vaslin, Guy Gogniat, Jean−Philippe Diguet, Russell Tessier, Wayne Burleson

Simulation Framework for Performance Prediction in the Engineering of Reconfigurable Systems and Applications 124
Eric Grobelny, Casey Reardon, Adam Jacobs, Alan George

FPGA Implementation of an Analytical Design Method for A Cycle−Optimal 2D−DCT/IDCT 131
Michaela Amoo, Clay Gloster, Jr.

Prototyping of a Two−Phase Micropipeline on FPGAs 138
Abdel Ejnioui

SESSION: RECONFIGURABLE HARDWARE

A New Routing Approach to Minimizing FPGA Reconfiguration Data 147
Weinan Chen, Chenglian Peng, Bo Zhou

Latency Optimization for a Reconfigurable, Self−Timed, and Bit−Serial Architecture 152
Florian Dittmann, Achim Rettberg, Raphael Weber

An FPGA Implementation of Reciprocal Sums for SPME 159
Sam Lee, Paul Chow
Optimization of Shared High–Performance Reconfigurable Computing Resources
Melissa Smith, Gregory Peterson

Computation Patterns Identification for Instruction Set Extensions Implemented as Reconfigurable Hardware
Christophe Wolinski, Krzysztof Kuchcinski

Critical Path Delay Reduction in FPGAs with Unbalanced Lookup Times
Jason Meyer, Fatih Kocan, Daniel Saab

SESSION: SHORT PAPERS

Reducing the reconfiguration overhead: a survey of techniques
Elena Perez–Ramo, Javier Resano, Daniel Mozos, Francky Catthoor

Implementing the G.723.1 Speech Codec Using a Coarse–Grained Reconfigurable Coprocessor
Henrik Svensson, Thomas Lenart, Viktor Öwall

Exploring Partial Reconfiguration for Mitigating SEU faults in SRAM–Based FPGAs
Cristiana Bolchini, Fabio Salice, Marco Domenico Santambrogio

Performance Analysis of Multi–process Execution Model on Dynamically Reconfigurable Processor
Vu Manh Tuan, Yohei Hasegawa, Hideharu Amano

Agent–Based Reconfigurability for Fault–Tolerance in Network–on–Chip
Pekka Rantala, Jouni Isoaho, Hannu Tenhunen

Design and Evaluation of a Software Infrastructure for the Runtime Management of Reconfigurable Resources
Dimitris Syrivelis, Spyros Lalis

Evolvable Hardware: A Functional Level Evolution Framework Based on ImpulseC
Anna Antola, Marco Castagna, Pamela Gotti, Marco Domenico Santambrogio

Autonomous Computing Systems: A Proposed Roadmap
Neil Steiner, Peter Athanas

SESSION: POSTERS

A TCP/IP Fragmentation Monitoring Core For Intrusion Prevention
Vukasin Pejovic, Slobodan Bojanic, Carlos Carreras
SESSION: LATE PAPERS

Pure ASIC-Based Retargetable Computing: Architectures, Advantages, and Challenges
Yong-Kyu Jung

Design of Homogeneous Communication Infrastructures for Partially Reconfigurable FPGAs
Jens Hagemeyer, Boris Kettelhoit, Markus Koester, Mario Porrmann

A Sandbox for Exploring the OpenFire Processor
Alex Marschner, Stephen Craven, Peter Athanas

Power Efficient Domain-Specific Reconfigurable Architectures for System-on-Chip Applications
Arjun K Pai, Khaled Benkrid

272 Gate Count Optically Differential Reconfigurable Gate Array VLSI
Minoru Watanabe, Takenori Shiki, Fuminori Kobayashi

FPGA Implementation of a Reconfigurable License Plate Detection Method
Ludek Bryan, Otto Fucik

Performance Evaluation of Two Allocation Schemes for Combinatorial Group Testing Fault Isolation
Rawad Al-Haddad, Carthik Sharma, Ronald DeMara

Efficient FPGA-based Implementation of Time Synchronization for MIMO-OFDM
Jeoong Sung Park, Hong-Jip Jung

High-Level Specification of Runtime Reconfigurable Designs
Stephen Craven, Peter Athanas

A Scalable and Reconfigurable Shared-Memory Graphics Cluster Architecture
Ross Brennan, Michael Manzke, Keith O'Conor, John Dingliana, Carol O'Sullivan

Optimization of Reconfiguration-speed Control Bits for an Optically Reconfigurable Gate Array
Minoru Watanabe

Feasibility of Hardware Acceleration of a Neocortex Model
Sébastien Lafontant, Tarek Taha

Autonomous Computing Systems: A Proof-of-Concept
Neil Steiner, Peter Athanas